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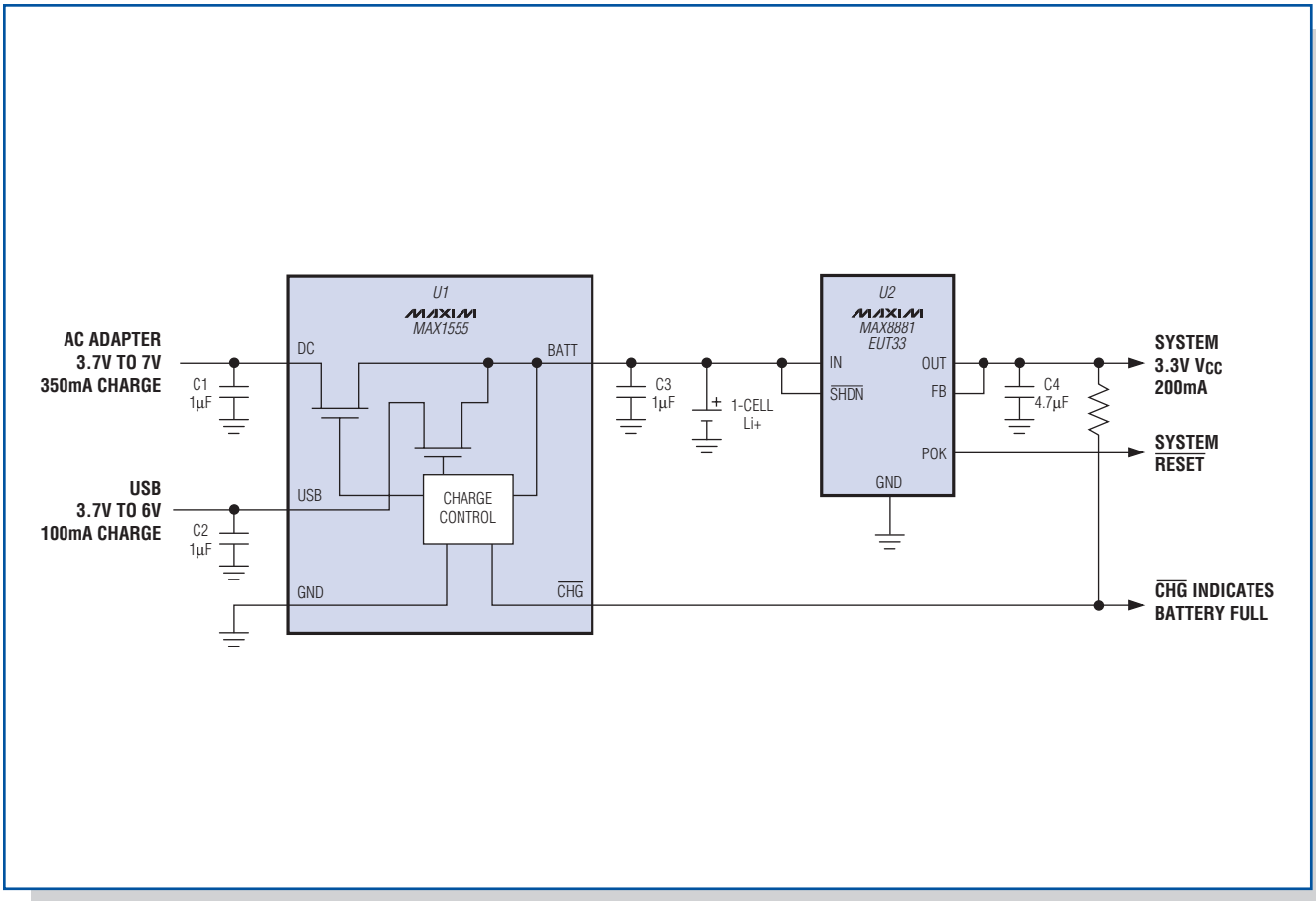

With simple charging at 100mA from USB and 350mA from an AC adapter, no enumeration is needed for the charger. (See article inside, page 8.)

News Briefs

MAXIM REPORTS REVENUES AND EARNINGS FOR THE THIRD QUARTER OF FISCAL 2004 AND DECLARES QUARTERLY DIVIDEND

Maxim Integrated Products, Inc., (MXIM) reported net revenues of $370.0 million for its fiscal third quarter ending March 27, 2004, a 29.3% increase over the $286.2 million reported for the third quarter of fiscal 2003 and a 9.4% increase over the $338.1 million reported for the second quarter of fiscal 2004. Net income for the quarter was $109.2 million, a 40.7% increase over the $77.6 million reported last year and a 10.8% increase over the $98.5 million reported for the second quarter. Diluted earnings per share were $0.31 for the third quarter, a 34.8% increase over the $0.23 reported for the same period a year ago and a 10.7% increase over the $0.28 reported for the second quarter of fiscal 2004.

During the quarter, the Company repurchased 8.0 million shares of its common stock for $385.1 million, paid dividends of $26.3 million, and acquired $69.8 million in capital equipment. During the fourth quarter of fiscal 2004 to date, the Company has repurchased an additional 2.1 million shares of its common stock for $100.1 million. Accounts receivable increased $29.0 million in the third quarter to $162.4 million primarily as a result of increased net revenues, and inventories decreased $4.9 million to $103.4 million.

Research and development expense was $77.3 million or 20.9% of net revenues in the third quarter, compared to $71.2 million or 21.1% of net revenues in the second quarter. The increase in research and development expense in the third quarter was due to hiring additional engineers and increased expenses to support the Company's new product development efforts. Selling, general and administrative expenses increased from $22.2 million in the second quarter to $23.5 million in the third quarter but decreased as a percentage of net revenues from 6.6% to 6.4%.

Third quarter bookings were approximately $488 million, a 17% increase over the second quarter's level of $417 million. Turns orders received in the quarter were approximately $189 million (turns orders are customer orders that are for delivery within the same quarter and may result in revenue within the same quarter if the Company has available inventory that matches those orders). Bookings increased in all geographic locations, with the greatest bookings improvement in Europe and the United States.

Third quarter ending backlog shippable within the next 12 months was approximately $437 million, including approximately $373 million requested for shipment in the fourth quarter of fiscal 2004. The Company's second quarter ending backlog shippable within the next 12 months was approximately $327 million, including approximately $293 million that was requested for shipment in the third quarter of fiscal 2004.

Jack Gifford, Chairman, President, and Chief Executive Officer, commented: "Bookings grew robustly in the third quarter, and orders for our power management products, telecom/datacom products, products for ATE and industrial applications, and other products serving an even broader base of customers were significantly above second quarter levels."

Mr. Gifford continued: "We are comfortable that capacity is in place or coming on line to meet forecasted demand for fiscal 2005. Start-up activities at our fab in San Antonio are proceeding on schedule, and we expect product for shipment to be manufactured at that facility in the fourth quarter. Our new test facility in Thailand will be in operation as planned in the first quarter of fiscal 2005, and we continue to increase capacity in both Thailand and the Philippines with additional equipment purchased over the past few quarters."

Mr. Gifford concluded: "The Company's Board of Directors has declared a quarterly cash dividend of $0.08 per share. Payment will be made on May 28, 2004 to stockholders of record on May 7, 2004."

Optical receiver performance evaluation

An essential parameter in determining the system power budget in an optical transmission system is optical receiver sensitivity, defined as the minimum average optical power for a given bit-error rate (BER). When designing a good optical receiver, it is critical to understand the different parameters that will impair overall receiver sensitivity. This article provides an in-depth analysis of complete receiver optical sensitivity and the potential power penalties related to the accumulation of random noise and intersymbol interference (ISI) in both amplitude and timing. The analysis is based on normal receiver sensitivity, assuming an ideal input signal with negligible impairment from factors like ISI, rise/fall time, jitter, and transmitter relative intensity noise (RIN).

Q-factor in the presence of ISI

A typical optical receiver is composed of an optical photo detector, a transimpedance amplifier, a limiting amplifier, and a clock-data recovery block. The simplified optical receiver model is shown in **Figure 1**.

The received optical signal is first converted into photocurrent and amplified by the transimpedance amplifier (TIA). The limiting amplifier acts as a "decision" circuit, where the sampled voltage v(t) is compared with the decision threshold V_{TH}. At this data decision point, the signal is significantly degraded by the accumulation of random noise and ISI, resulting in erroneous decisions due to eye closure.

To know the relationship between BER and eye opening at data decision, the statistical characteristics of the amplitude noise need to be determined. Usually, as a figure of merit, we use signal Q-factor to measure the signal quality for determining the BER. If the ISI distortion does not exist and the dominant amplitude noise has Gaussian distribution, the signal Q-factor is defined as:

$$Q = \frac{V_1 - V_0}{\sigma_1 - \sigma_0} \qquad \text{(Eq 1)}$$

Here V_1, V_0 are the mean values for v(t) amplitude high and low without ISI, while σ_1, σ_0 are the root mean square (RMS) of the additive white noise for each Gaussian distribution. For a detailed description, please refer to the MAXIM® application note, *HFAN-09.0.2 Optical Signal-to-Noise Ratio and the Q-factor in Fiber-Optic Communications Systems.* (www.maxim-ic.com/AN985)

In a practical receiver implementation, ISI exists due to receiver bandwidth limitation, baseline wander, or nonlinearity of the active components. If we monitor the signal eye diagram before the data decision, we find that, in addition to random noise, the signal has a certain amount of bounded amplitude fluctuation caused by ISI, which exhibits strong pattern dependence. To estimate the ISI penalty on optical sensitivity, a simple solution is to consider a worst-case amplitude-noise distribution. This is done separately by shifting the mean value of the Gaussian distribution from V_1 and V_0 to the lower amplitude boundary (V_1 - V_{ISI}) and (V_0 + V_{ISI}). It is assumed that V_{ISI} is the vertical eye closure caused by ISI **(Figure 2)**.

Under this condition, the signal Q-factor can be obtained by calculating the BER from the worst-case noise distribution. Assuming the decision threshold is optimized for minimum BER, the Q-factor is related to vertical eye closure V_{ISI} as follows:

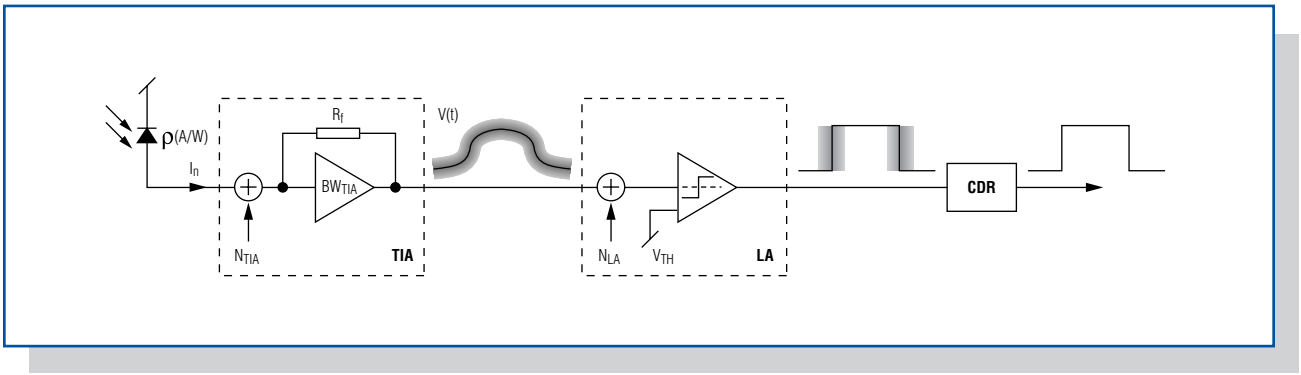

Figure 1. This diagram illustrates a simplified optical receiver model.

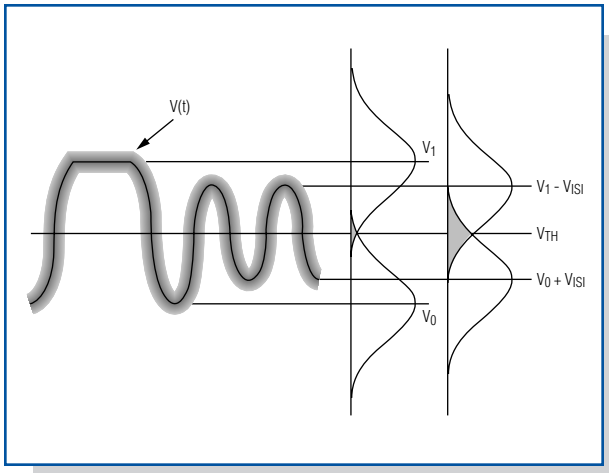

Figure 2. Worst-case amplitude-noise distribution in the presence of ISI facilitates estimation of the ISI penalty on optical sensitivity.

$$Q = \frac{V_1 - V_0 - 2 \times V_{ISI}}{\sigma_1 + \sigma_0} \qquad \text{(Eq 2)}$$

$$BER = \frac{1}{2}\operatorname{erfc}\left(\frac{Q_{BER}}{\sqrt{2}}\right) \qquad \text{(Eq 3)}$$

Where: $$\operatorname{erfc}(x) = \frac{2}{\sqrt{\pi}}\int_x^{\infty} e^{-v^2} dv$$

Q_{BER} is the minimum required Q-factor for a given BER. Based on equation 3, the relationship between Q_{BER} and BER is plotted in **Figure 3**.

Usually we measure the signal peak-to-peak differential swing ($V_{P-P} = V_1 - V_0$) in the lab and assume $\sigma_1 = \sigma_0 = N_{RMS}$, so the Q-factor becomes:

$$Q = \frac{V_{P-P} - 2 \times V_{ISI}}{2 \times N_{RMS}} \qquad \text{(Eq 4)}$$

Here N_{RMS} is the equivalent RMS noise at the input of the limiting amplifier. Equation 4 demonstrates that Q-factor is a measure of the vertical eye opening to RMS noise ratio in the presence of ISI. The Q-factor reduction due to ISI causes optical power penalty or error floor in an optical receiver design.

Optical sensitivity estimation

To achieve the best optical sensitivity, it is important to maximize the signal Q-factor before data decision. The following section demonstrates how to accurately estimate the receiver optical sensitivity with practical device implementations, when overall receiver random noise, ISI, and CDR jitter tolerance are taken into account. Examples are given for both a 10Gbps receiver and a 2.5Gbps receiver using MAXIM devices.

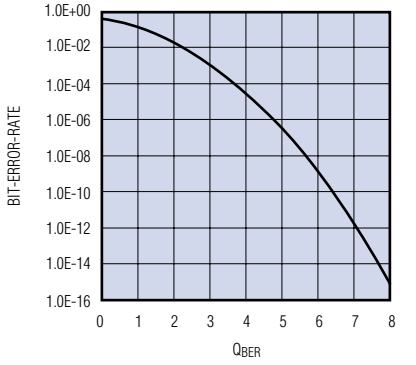

Figure 3. BER vs. QBER is plotted based on equation 3.

Overall receiver RMS noise penalty

To estimate the receiver total RMS noise impact on optical sensitivity, we must know the minimum required peak-to-peak current at the TIA input (noted as I_{P-P}) that will result in a specified BER. For this random noise analysis it is assumed $V_{ISI} = 0$, and I_{P-P} can be obtained by substituting $V_{P-P} = I_{P-P} \times R_f$ and $N_{RMS} = N_{TOTAL} \times R_f$ in equation 4, resulting in:

$$I_{P-P} = 2 \times Q_{BER} \times N_{TOTAL}\ (\mu A_{RMS}) \qquad \text{(Eq 5)}$$

N_{TOTAL} is the total equivalent RMS noise at TIA input, which is determined by the TIA input-referred noise N_{TIA} (μA_{RMS}), the limiting-amplifier input-referred noise N_{LA} (mV_{RMS}), and the TIA small-signal transimpedance gain R_f ($k\Omega$). The relationship is shown as:

$$N_{TOTAL} = \sqrt{N_{TIA}^2 + \left(\frac{N_{LA}}{R_f}\right)^2} \qquad \text{(Eq 6)}$$

In practice, the limiting-amplifier (LA) input-referred noise may not be given, but N_{LA} can be estimated from the limiting-amplifier input-sensitivity V_{LA}, a measure of the minimum differential peak-to-peak signal swing to achieve a given BER. In general, the limiting-amplifier sensitivity could result from the input-referred noise N_{LA}, DC-offset, or ISI due to bandwidth limitation. However, since most limiting amplifiers implement a DC-offset cancellation loop for high sensitivity, and the small-signal bandwidth is usually much higher than that of the TIA, we can assume that the random noise is the dominant factor for limiting amplifier sensitivity. Under this condition, N_{LA} can be estimated from the following equation:

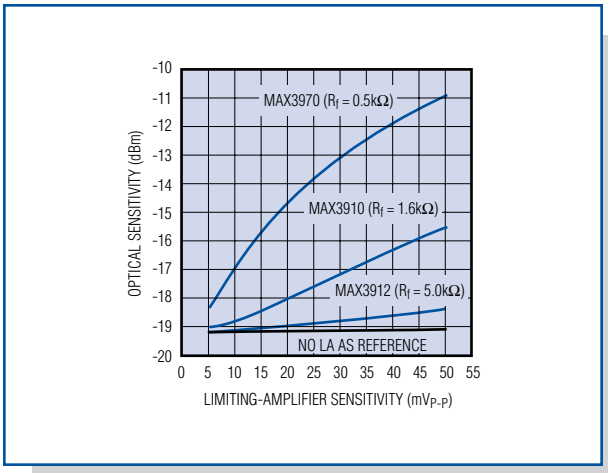

Figure 4. Receiver optical sensitivity is shown for 10Gbps TIA ICs, assuming the SONET minimum extinction-ratio requirement.

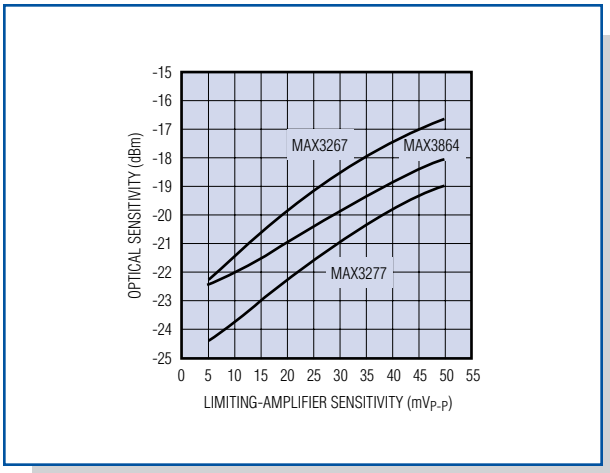

Figure 5. This graph shows the receiver optical sensitivity for 2.5Gbps TIA ICs when each is used with a limiting amplifier of different sensitivity.

$$N_{LA} = \frac{V_{LA}}{2 \times Q_{BER}} \qquad \text{(Eq 7)}$$

According to Figure 3, $Q_{BER} = 7$ for BER = 10^{-12}. Assuming ρ is the photo detector responsivity (A/W), and r_e is the extinction ratio of the received optical signal, the optical modulation amplitude (OMA) is obtained as:

$$OMA = \frac{I_{P-P}}{\rho} (\mu W) \qquad \text{(Eq 8)}$$

Optical sensitivity is given by:

$$P_{ave} (dBm) = 10 \log\left(\frac{OMA}{2 \times 1000} \times \frac{r_e + 1}{r_e - 1} \right) \qquad \text{(Eq 9)}$$

The MAX3970, MAX3910, and MAX3912, for example, are 10Gbps TIA ICs with typical input-referred noise of $1.1\mu A_{RMS}$, but with different transimpedance gain. When each of these devices is used in conjunction with a limiting amplifier of different sensitivities, the achieved optical sensitivity of the complete receiver differs. Assuming ρ = 0.85A/W and $r_e = 6.6$ (SONET minimum extinction-ratio requirement), the calculated optical sensitivity is shown in **Figure 4**.

If we use the optical sensitivity obtained from the TIA input-referred noise as a reference without a LA, the optical power penalty caused by total receiver random noise is the difference between the reference and the combination of TIA with limiting amplifier. For example, the MAX3971 is a 10Gbps limiting amplifier with input sensitivity of $9.5mV_{P-P}$ for BER ≤ 10^{-12}. When the MAX3970 TIA is used together with MAX3971, the optical power penalty is about 2.1dB. When the MAX3912 TIA is used with MAX3971, however, the optical penalty is only 0.03dB.

Another example is the 2.5Gbps SFP receiver module, which consists of an optical photo detector and a 2.5Gbps TIA followed by a limiting amplifier. For this application, MAXIM provides a series of TIA ICs such as the MAX3267, MAX3271, MAX3275, MAX3277, and MAX3864. **Figure 5** shows the optical sensitivity for the MAX3267 ($N_{TIA} = 0.495\mu A_{RMS}$, $R_f = 1.9k\Omega$), MAX3864 ($N_{TIA} = 0.49\mu A_{RMS}$, $R_f = 2.75k\Omega$), and MAX3277 ($N_{TIA} = 0.3\mu A_{RMS}$, $R_f = 3.3k\Omega$) when each of these devices is used together with a limiting amplifier of different sensitivity.

Choices for 2.5Gbps limiting amplifiers are the MAX3265, MAX3269, MAX3272, MAX3765, MAX3861, and MAX3748. The user can choose different TIA and limiting-amplifier combinations for use in different SFP modules, depending on performance, cost, or package needs.

Intersymbol interference penalty

In an optical receiver, ISI can result from the following sources: high-frequency bandwidth limitation; insufficient low-frequency cutoff caused by AC-coupling or DC-offset cancellation loop; in-band gain flatness; or multiple reflection between the interconnection of a TIA and a limiting amplifier. Depending on the nature of the data pattern being received (e.g., PRBS 2^{31}- 1, K28.5, 8B/10B encoding), the ISI distortion could differ. ISI results in eye closure in both amplitude and timing.

If we define the ISI due to vertical eye closure as:

$$ISI = \frac{2 \times V_{ISI}}{V_{P-P}} \qquad \text{(Eq 10)}$$

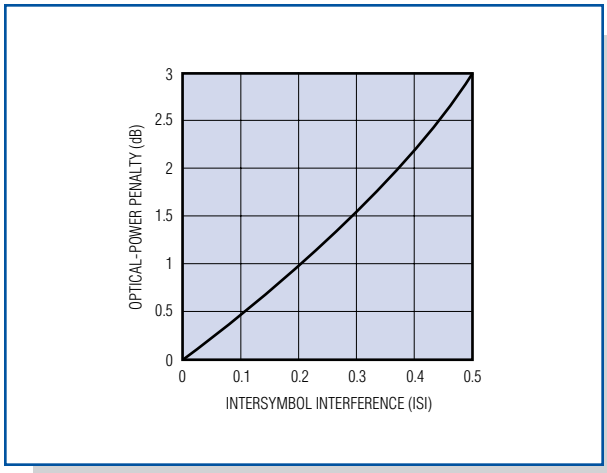

Figure 6. The relationship between ISI and optical power penalty in an ideal case is illustrated.

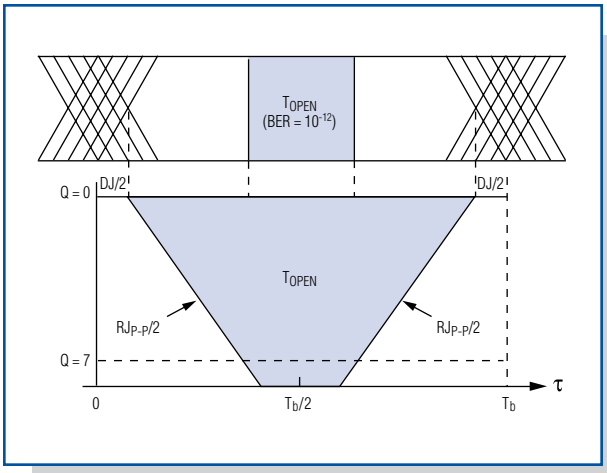

Figure 7. This illustrates the relationship between CDR minimum eye opening and the Q-factor.

The minimum-required TIA input current is related to ISI according to:

$$I_{P-P} = \frac{2 \times Q_{BER} \times N_{TOTAL}}{(1 - ISI)} \qquad \text{(Eq 11)}$$

The ISI penalty is defined as the difference in optical sensitivity in the presence of ISI, as compared to an ideal case when ISI = 0. The calculated result is shown in **Figure 6**. The optical power penalty is 0.46dB for 10% ISI distortion.

Finally, the total optical power penalty in dB is the sum of the ISI penalty and the overall random-noise penalty.

CDR jitter-tolerance penalty

As the signal goes through the receiver amplifier chain to the limiting stage, the amplitude noise is converted into timing jitter at the data midpoint crossing. Random and deterministic jitter are generated due to the existence of random noise, limited bandwidth, passband ripple, group-delay variation, AC-coupling, and nonsymmetrical rise/fall times. The combination of these jitter components decreases the eye opening available for error-free data recovery. Consequently, CDR jitter-tolerance capability is another critical factor for determining optical sensitivity.

CDR jitter tolerance is a measure of how much peak-to-peak jitter can be added to the incoming data before errors occur due to misalignment of the data and recovered clock. For a PLL-based CDR design, a minimum data-eye opening is required, which is determined by the clock-to-data sampling position, the retiming flip-flop setup/hold times, and the phase detector characteristics. Assuming that the random jitter is RJ_{RMS}, the total deterministic jitter is DJ_{P-P}, and the CDR minimum required eye opening is T_{OPEN} at a specified BER, then the timing Q-factor is defined as:

$$Q = \frac{T_b - T_{OPEN} - DJ_{P-P}}{2 \times RJ_{RMS}} \qquad \text{(Eq 12)}$$

$$RJ_{P-P} = 2Q_{BER} \times RJ_{RMS} \qquad \text{(Eq 13)}$$

For more information, refer to application note *HFAN-04.0.2 Converting between RMS and Peak-to-Peak Jitter at a Specified BER.* (www.maxim-ic.com/AN337)

The relationship between the CDR minimum eye-opening requirement and the Q-factor is illustrated in **Figure 7**. To achieve a specified BER, the corresponding minimum Q_{BER} can be found from Figure 3.

When the jitter frequency at the CDR input is higher than the PLL bandwidth, the CDR jitter tolerance (noted as JT_{P-P}) is related to T_{OPEN} as:

$$JT_{P-P} = (T_b - T_{OPEN}) \qquad \text{(Eq 14)}$$

To avoid degrading the optical sensitivity, the CDR high-frequency jitter tolerance should satisfy:

$$JT_{P-P} \geq 2 \times Q_{BER} \times RJ_{RMS} + DJ_{P-P} \qquad \text{(Eq 15)}$$

Depending on the slope of the edge transition, the random jitter RJ_{RMS} is generated from the additive white noise at signal transitions. Assuming that the signal rise/fall time (20% to 80%) before limiting is symmetrical and equal to t_r, the random jitter can be estimated by:

$$RJ_{RMS} = \frac{t_r}{(V_{P-P}/N_{RMS}) \times 0.6} \qquad \text{(Eq 16)}$$

Here t_r is dependent on the overall receiver small-signal bandwidth BW_{TOTAL}. Assuming a first-order lowpass filter:

$$t_r \approx \frac{0.22}{BW_{TOTAL}} \qquad \text{(Eq 17)}$$

At the optical receiver input, it is assumed that the TIA is linear before the limiting amplifier. Therefore, random jitter can be expressed as a function of the peak-to-peak current to the total RMS noise ratio at TIA input:

$$RJ_{RMS} = \frac{t_r}{(I_{P\text{-}P}/N_{TOTAL}) \times 0.6} \qquad \text{(Eq 18)}$$

Using Equation 18, the random jitter at the limiting-amplifier output is plotted in **Figure 8** as a function of TIA input current to noise ratio.

The CDR jitter-tolerance penalty on optical sensitivity can be estimated by combining equations 15 and 18, then solving for $I_{P\text{-}P}$ as:

$$I_{P\text{-}P} = \frac{2 \times Q_{BER} \times t_r}{(JT_{P\text{-}P} - DJ_{P\text{-}P}) \times 0.6/N_{TOTAL}} \qquad \text{(Eq 19)}$$

Again we take the OC-192 receiver as an example. Assuming ρ = 0.85A/W and r_e = 6.6, the total receiver small-signal bandwidth is 7.0GHz, N_{TOTAL} = 1.1μA_{RMS}, and ISI = 0. **Figure 9** shows the optical sensitivity achievable with different CDR jitter tolerance (BER = 10^{-12}).

In general, to achieve a specified BER, the minimum TIA input current should satisfy the Q_{BER} in both amplitude and timing.

Conclusion

To estimate optical-receiver sensitivity, it is necessary to consider error sources in both amplitude and timing. This article shows how the amplitude and timing-error sources separately affect the overall receiver BER with practical device implementations. Using these guidelines, optical receiver performance can now be accurately predicted to choose the proper TIA, limiting amplifier, and CDR. In reality, the optical input is not an ideal signal, because it suffers random noise from the transmitter as well as ISI from fiber dispersion. When a stressed optical signal is received, the same approach presented in this article can be used for estimating the signal Q-factor and, therefore, determining the BER.

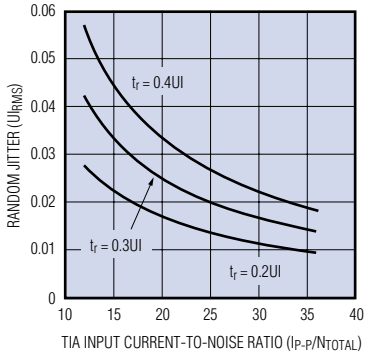

Figure 8. Random jitter and input-current-to-noise ratios are shown for rise times of 0.2UI, 0.3UI, and 0.4UI.

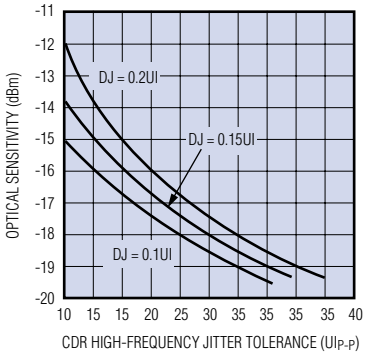

Figure 9. The relationship between optical sensitivity and CDR jitter tolerance is illustrated for deterministic jitter tolerances of 0.1UI, 0.15UI, and 0.2UI.

USB battery charging

One of the best, but least celebrated, features of the USB standard is the power supplied from the host to plugged-in USB peripherals. This enlightened change from the serial and parallel ports of the past allows a dramatic increase in the variety of devices that can be conveniently connected to a PC.

Besides directly powering USB devices, one of the more useful functions that can be performed with USB power is battery charging. Because many portable devices, such as MP3 players and PDAs, exchange information with PCs, device convenience is significantly enhanced if battery charging and data exchange take place simultaneously and over one cable. Combining USB and battery-powered functionality gives rise to a whole range of untethered devices like removable web cameras that operate whether or not connected to a PC. In many cases, it is no longer necessary to include the ever-present and awkward AC adapter.*

Battery charging from USB can be complex or straight forward, as dictated by the demands of the USB device. Design influences range beyond the typical chorus of cost, size, and weight. Other key considerations include: 1) how quickly a device with a discharged battery must operate with full functionality when plugged into a USB port; 2) the time that can be allowed for battery charging; 3) power budgeting within USB limits; and 4) the necessity of including AC adapter charging. These issues and their solutions will be addressed after some discussion of USB from a power point of view.

USB power

All USB host devices, like PCs and notebooks, can source at least 500mA or five "unit loads" per USB socket. In USB terminology, "one unit load" is 100mA. Self-powered USB hubs can also supply five unit loads. Bus-powered USB hubs are guaranteed to supply only one unit load. According to the USB spec illustrated in **Figure 1**, the minimum available voltage from a USB host or powered hub at the peripheral end of the cable is 4.5V, while the minimum voltage from a USB bus-powered hub is 4.35V. These voltages allow very little headroom when charging Li+ batteries that typically require 4.2V, making charger dropout extremely important.

All devices that plug into a USB port must start out drawing no more than 100mA. After communicating with the host, the device can determine if it can take the full 500mA.

USB peripheral devices contain one of two receptacles. Both are smaller than the socket found in PCs and other USB hosts. The "Series B" and the smaller "Series Mini-B" receptacles are shown in **Figure 2**. Power is taken from pins 1 (+5V) and 4 (GND) on the Series B, and from pins 1 (+5V) and 5 (GND) on the Series Mini-B.

Once connected, all USB devices must identify themselves to the host. This is called enumeration. There are practical exceptions to this rule that will be discussed at the end of this article. In the identification process, the host determines the power needs of the USB devices and gives, or denies, the approval for the device to increase its load from 100mA (max) to 500mA (max).

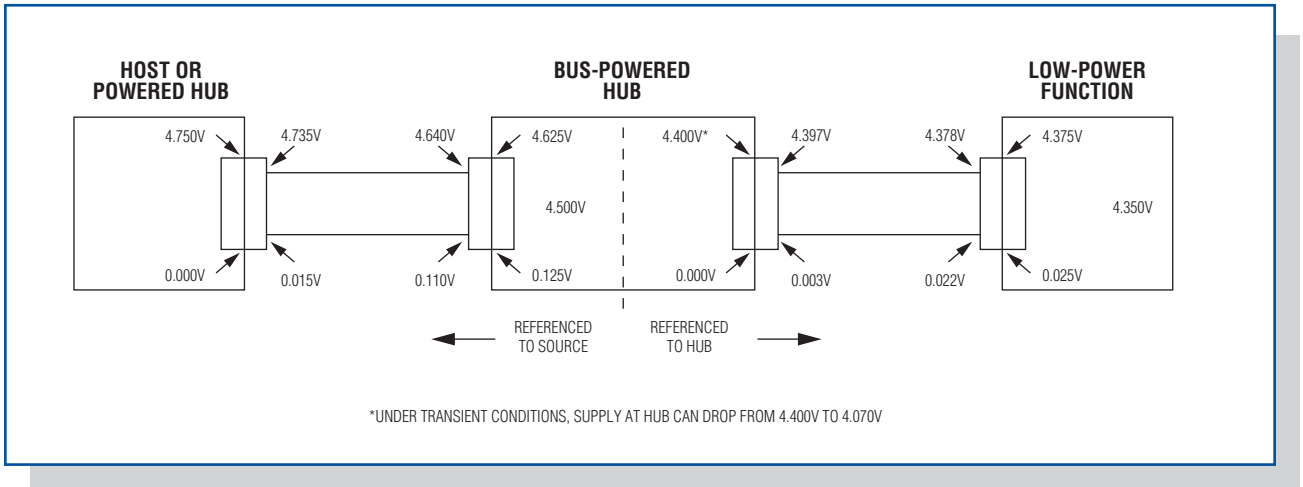

Figure 1. This diagram shows USB voltage drops from Universal Serial Bus Specification Rev 2.0.

**Maxim Integrated Products, Inc. holds a US patent (6,507,172) on all forms of USB Li+ battery charging.*

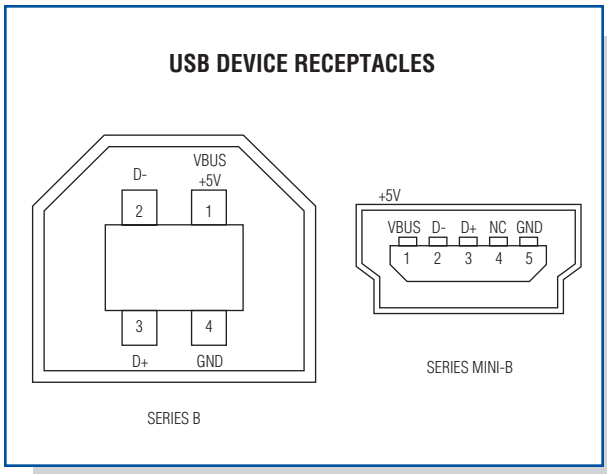

Figure 2. These receptacles for USB peripherals differ from the large four-pin sockets found on hosts and hubs. Power and data connection pins are shown.

Simple USB/AC adapter charging

Some very basic devices many not require the software overhead needed to sort out and optimize use of the available USB power. If the device's load current is limited to 100mA, any USB host, self-powered hub, or bus-powered hub can power the device. For such designs, a very basic charger and regulator scheme is shown in **Figure 3**.

The circuit in Figure 3 charges the battery whenever the device is docked to USB or plugged into the AC adapter. At the same time, the system load is always connected to the battery, in this case through a simple linear regulator (U2), which can supply up to 200mA. If the system continuously draws that amount of current while the battery is charging at 100mA from USB, the battery will still discharge as the load current exceeds the charge current. In most small systems, the peak loads occur only for a fraction of the total operating time. Therefore, as long as the average load current is less than charging current, the battery will still charge. When the AC adapter is connected, the charger's (U1) maximum current increases to 350mA. If USB and the AC adapter are connected at the same time, the AC adapter is automatically given precedence.

One characteristic of U1 *required* by the USB spec (but also wise for chargers in general) is that current never be allowed to flow back to a power input from either the battery or another power input. In conventional chargers this can be guaranteed with input diodes, but the small difference between the minimum USB voltage (4.35V) and the required Li+ battery voltage (4.2V) makes even Schottky diodes inappropriate. For this reason, all reverse-current paths are blocked within the U1 IC.

The circuit of Figure 2 has limitations that may make it inappropriate for some rechargeable USB devices. The most obvious limitation is its relatively low charge current, which translates to long charge time if the Li+ battery capacity is more than a few hundred milli-amp hours. The second limitation occurs because the load (linear regulator input) is always connected to the battery. In this case, the system may not be able to operate immediately upon being plugged in if the battery is deeply discharged. This happens because there may be a delay before the battery reaches a sufficient voltage for the system to operate.

Load switching and other enhancements

In more advanced systems, a number of enhancements are often required in or around the charger. These can

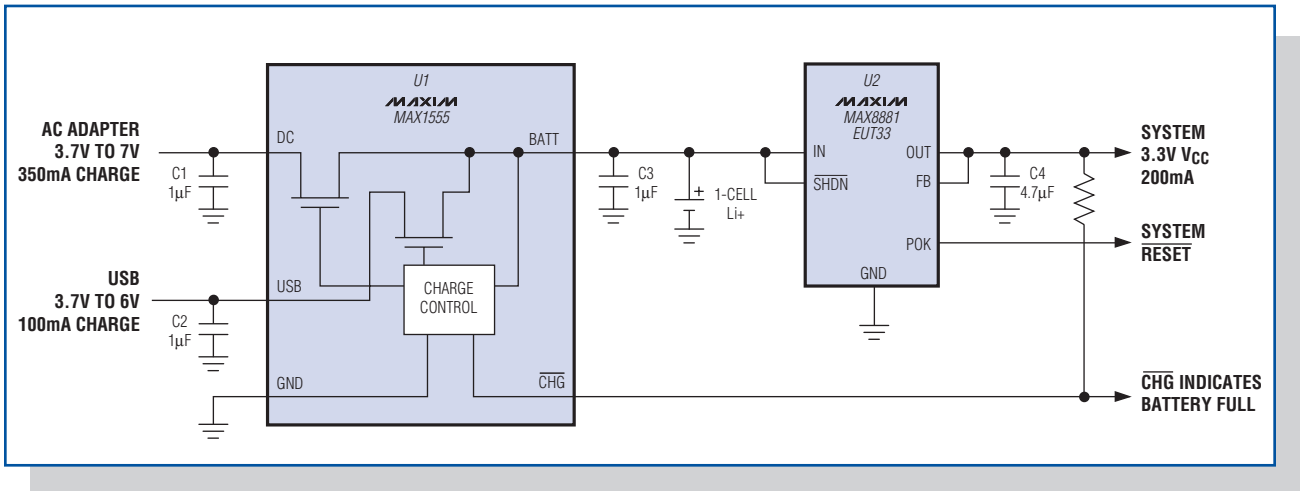

Figure 3. With simple charging at 100mA from USB and 350mA from an AC adapter, no enumeration is needed for the charger, because the USB charge current does not exceed one unit load (100mA). The 3.3V system load is always drawn from the battery.

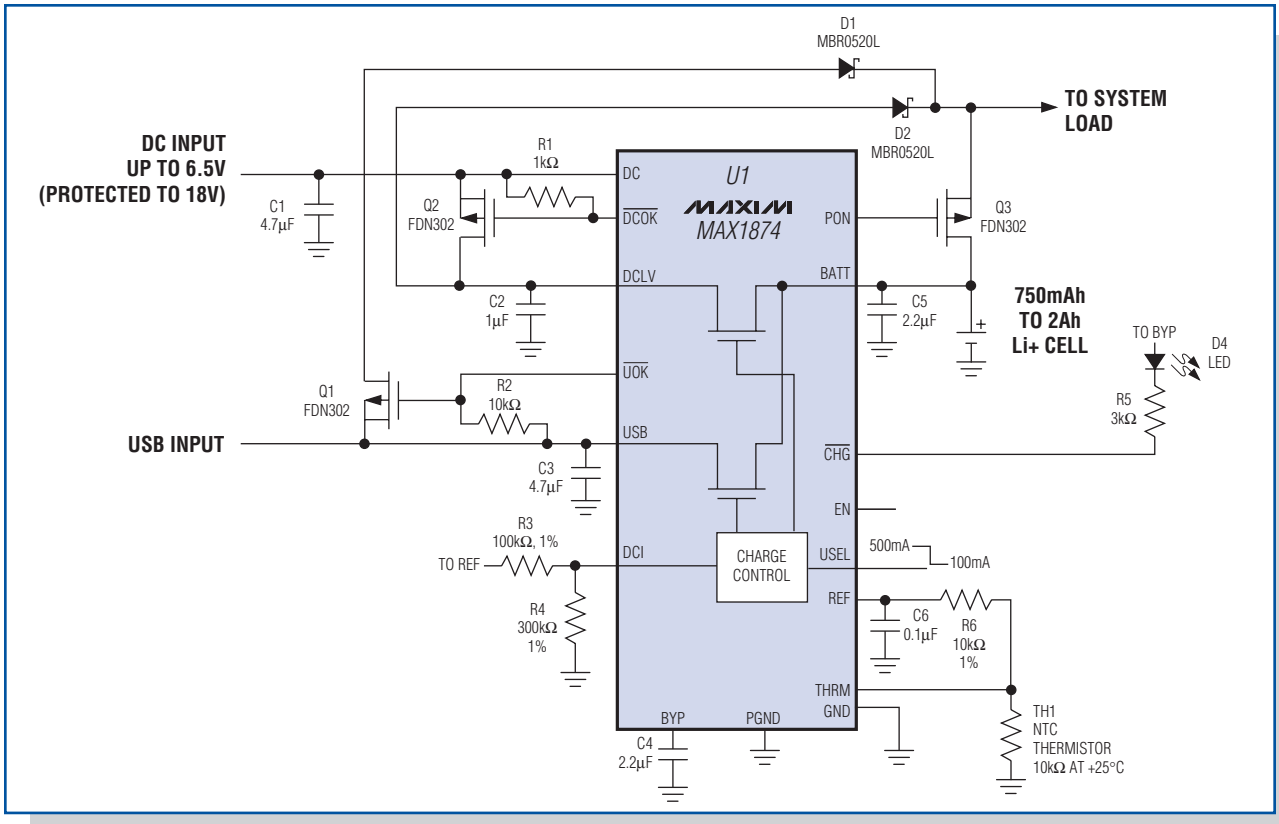

Figure 4. SOT23 power MOSFETs add useful features such as overvoltage protection and battery disconnect when external power is applied. The active power source drives the system directly while the battery charges unload.

include: selectable charge current to match the current capability of the source (USB or AC adapter) or battery; load switching when power is plugged in; and overvoltage protection. The circuit in **Figure 4** adds some of these features by means of external MOSFETs driven by voltage detectors in the charger IC.

MOSFETs Q1 and Q2 and diodes D1 and D2 bypass the battery and connect the active (USB or AC-adapter) power input directly to the load. When a power input is valid, its monitor output ($\overline{UOK}$ or $\overline{DCOK}$) goes low to turn on the appropriate MOSFET. When both inputs are valid, the DC input has precedence; U1 prevents both inputs from being active at the same time. Diodes D1 and D2 prevent reverse current from flowing between inputs through the system-load power path, while the charger has built-in circuitry to prevent reverse current through the charging path (at BATT).

MOSFET Q2 also provides AC-adapter overvoltage protection up to 18V. An under-/overvoltage monitor (at DC) allows charging only when the AC adapter voltage is between 4V and 6.25V.

The last MOSFET, Q3, turns on to connect the battery to the load when no valid external power is present. When either USB or DC power is connected, the power on (PON) output immediately shuts off Q3 to disconnect the battery from the load. This allows the system to operate immediately when external power is applied, even if the battery is deeply discharged or damaged.

When USB is connected, the USB device communicates with the host to determine if the load current can be increased. The load starts out at one unit load and is increased to five unit loads if the host allows it. This 5-to-1 current range can be problematic for conventional chargers not designed for USB. The problem is that the current accuracy of conventional chargers, though adequate at high current, usually suffers at low-current settings due to offsets in the current-sense circuitry. The result can be that the low-range (for one unit load) charge current must be set too low to be useful in order to be certain that it never exceeds the 100mA limit. For example, with 10% accuracy at 500mA, the output would have to be set for 450mA to ensure it never exceeds 500mA. That alone is acceptable; however, to ensure that the low-range charge current does not exceed 100mA, the nominal current would have to be set at 50mA. The minimum could then be 0mA, but that is clearly unacceptable. If USB charging is to be effective in both ranges,

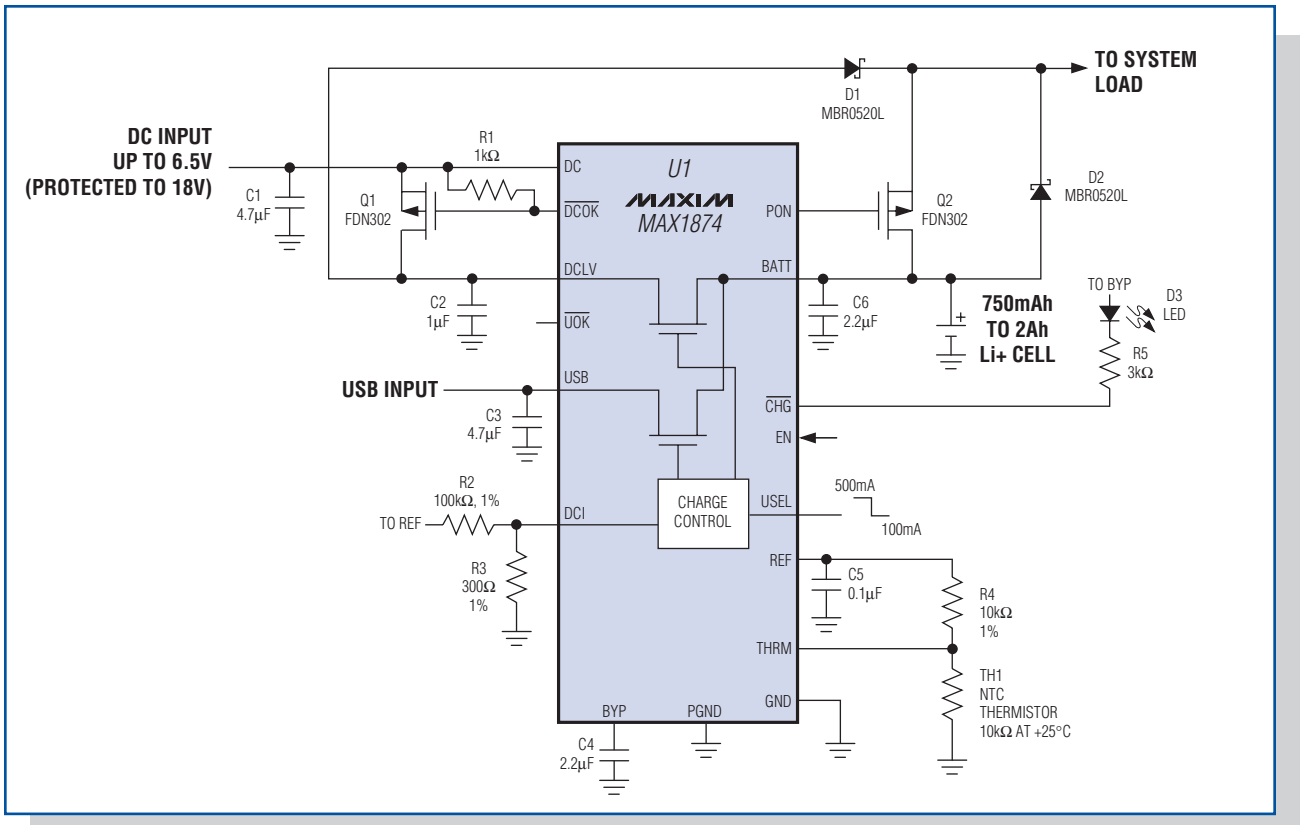

Figure 5. A simplified design does not pass USB power to directly to the load, but does so for the DC input. When USB is connected, the system is still powered, but from the battery while it also is charging.

sufficient accuracy is needed to allow the maximum-possible typical charge current without exceeding the USB limits.

In some designs the system-power needs make it impractical to separately power the load and charge the battery with less than the 500mA USB budget. Doing so, however, from an AC adapter is not a problem. The connection in **Figure 5**, a simplified subset of Figure 4, accomplishes this in a cost-effective way. USB power is not routed directly to the load; both charging and system operation still take place on USB power, but the system remains connected to the battery. The limitation in this design is the same as in Figure 3—if the battery is deeply discharged when USB is connected, there may be a delay before the system can operate. But, if DC power is connected, Figure 5 operates in the same manner as Figure 4 with no wait regardless of battery state. This is because Q2 turns off, passing the system load from the battery to the DC input through D1.

Nickel-metal hydride charging

Though Li+ batteries provide the best performance for most portable information devices, nickel-metal hydride (NiMH) cells can still be a viable choice in minimum-cost designs. A good way to keep costs low when the load requirements are not too severe is by using one NiMH cell. This requires a DC-DC converter to boost the typically 1.3V cell voltage into something the device can use, typically 3.3V. Because some type of regulator is needed for any battery-powered device, the DC-DC converter is really only a different regulator, not an additional one.

The connection in **Figure 6** uses an unusual approach to charge the NiMH cell and switch the system load between the USB input and battery with no external FETs. The "charger" is actually a DC-DC step-down converter (U1) operated in current limit. It charges the battery with 300mA to 400mA. Though not a precise current source, it has adequate current control for the purpose and is able to maintain current control even into a shorted cell. A big advantage of the DC-DC charging topology over more common linear schemes is efficient utilization of the limited USB power resource. When charging one NiMH cell at 400mA, the circuit draws only 150mA from the USB input. That leaves 350mA for system use while charging.

Load handoff from the battery to USB is accomplished by diode OR-ing (D1) USB power with the boost converter

output. When USB is disconnected, the boost converter generates 3.3V at the output. With USB connected, D1 pulls the DC-DC boost converter (U2) output up to approximately 4.7V. When U2's output is pulled up this way, it automatically turns off and draws less than 1µA from the battery. If the shift of the output from 3.3V to 4.7V output when USB is connected is not acceptable, then a linear regulator can be inserted in series with D1.

A limitation of this circuit is that it relies on the system to control charge termination. U1 acts only as a current source and will overcharge the cell if left on indefinitely. R1 and R2 set U1's maximum output voltage at 2V as a safety limit. The charge-enable input functions as a means for the system to terminate charging. It additionally functions as a way to reduce USB load current prior to enumeration, if necessary, because the charger's 150mA input current is more than one unit load.

What your mom didn't tell you about USB

With any standard, it is interesting to see how actual practice diverges from the printed specification, or how undefined parts of the specification take shape. Though USB is, with little doubt, one of the best thought out, reliable, and useful standards efforts in quite some time, it has not been immune to the impact of the real world. Here are some observed USB characteristics that may not be obvious, yet can influence power designs.

USB ports do NOT limit current. Though the USB spec provides details about how much current a USB port *must* supply, there are mile-wide limits on how much it *might* supply. Though the upper limit specifies that the current never exceed 5A, a wise designer should not rely on that information. In any case, a USB port can never be counted on to limit its output current to 500mA, or any amount near that. In fact, output current from a port often exceeds several amps, as multiport systems (like PCs) frequently have only one protection device for all ports in the system. The protection device is set above the *total* power rating of all the ports. Therefore, a four-port system may supply over 2A from one port if the other ports are not loaded. Furthermore, while some PCs use 10% to 20% accurate IC-based protection, others use much less accurate poly-fuses (fuses that reset themselves) that will not trip until the load is 100% or more above the rating.

USB ports rarely (never) turn off power. The USB spec is not specific about this, but sometimes it is thought that USB power may be disconnected as a result of failed enumeration or other software or firmware problems. In actual practice, no USB host shuts off USB power for anything other that an electrical fault (like a short). There may an exception to this statement, but it has yet to be seen. Notebook and motherboard makers are barely willing to pay for fault protection, let alone smart power switching. So no matter what dialog does or does not take place between a USB peripheral and host, 5V will be available (at either 500mA or 100mA, or maybe 2A or more). The appearance of USB-powered reading lights, coffee mug warmers, and similar items that have no communication capability illustrate this point. They may not be "compliant," but they do function.

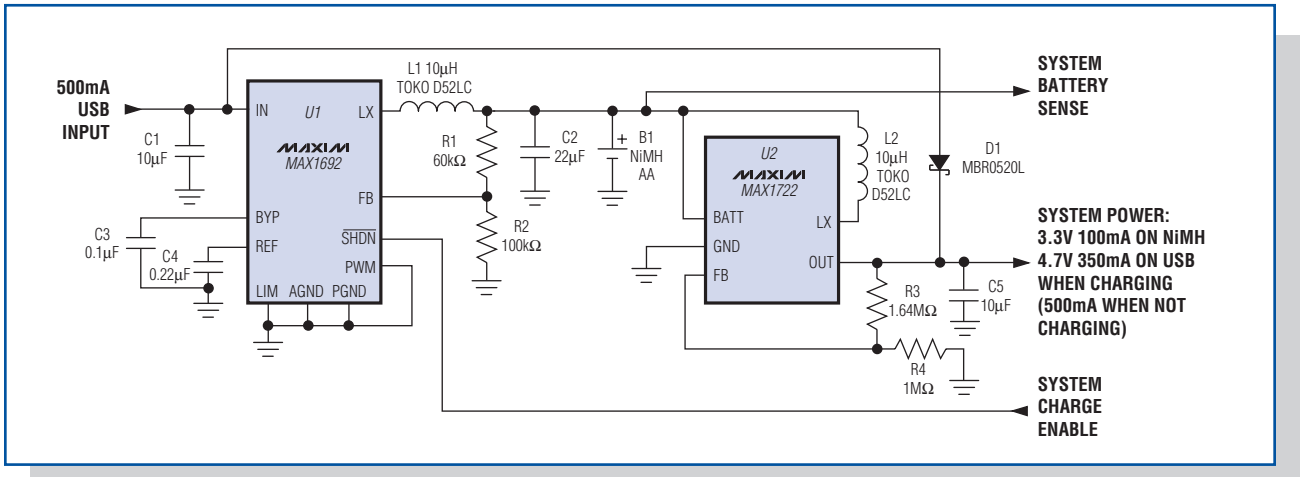

Figure 6. A simple NiMH charge/power-supply arrangement automatically hands off power to USB without a complex MOSFET switch array.

Logic-level translation

Electronic design has changed considerably since the days when TTL and 5V CMOS were the dominant standards for logic circuits. The increasing complexity of modern electronic systems has led to lower voltage logic, which in turn can cause incompatibility between input and output levels for the logic families within a system. It is not unusual, for example, that a digital section operating at 1.8V must communicate with an analog subsection operating at 3.3V. This article examines the basics of logic operation and considers, primarily for serial-data systems, the available methods for translating between different domains of logic voltage.

The need for logic-level translation

The growth of digital ICs that feature incompatible voltage rails, lower V_{DD} rails, or dual rails for V_{CORE} and $V_{I/O}$ has made the translation of logic levels necessary. The use of mixed-signal ICs with lower supply voltages that have not kept pace with those of their digital counterparts also creates the need for logic-level translation.

Translation methods vary according to the range of voltages encountered, the number of lines to be translated (e.g., a 4-line Serial Peripheral Interface (SPI™) versus a 32-bit data bus), and the speed of the digital signals. Many logic ICs can translate from high to low levels (such as 5V to 3.3V logic), but fewer can translate from low to high (3.3V to 5V). Level translation can be accomplished with single discrete transistors or even with a resistor-diode combination, but the parasitic capacitance inherent in these methods can reduce the data-transfer rate.

Although byte-wide and word-wide level translators are available, they are not optimal for the <20Mbps serial buses discussed in this article (SPI, I²C™, USB, etc.). Thus, translators that require large packages with high pin counts and an I/O-direction pin are not meant for small serial and peripheral interfaces.

The Serial Peripheral Interface consists of the unidirectional control lines data in, data out, clock, and chip select. Data in and data out are also known as master in, slave out (MISO) and master out, slave in (MOSI). SPI can be clocked in excess of 20Mbps, and is driven by CMOS push-pull logic. As SPI is unidirectional, translation in both directions on the same signal line is unnecessary. This makes level translation simpler, because you can employ simple techniques involving resistors and diodes (**Figure 1**) or discrete/digital transistors (**Figure 2**).

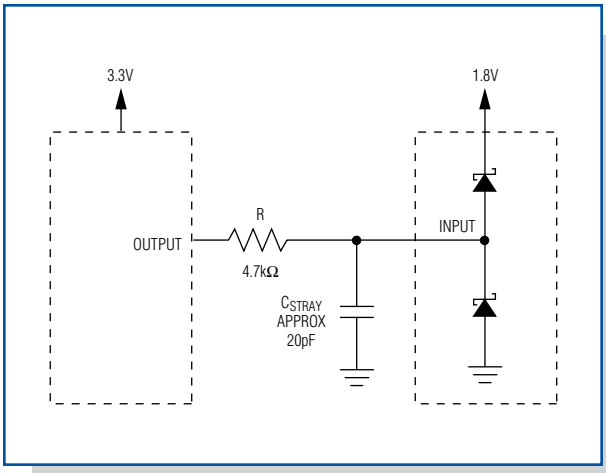

Figure 1. A resistor-diode topology is one alternative technique to translation in both directions on the same signal line.

The I²C, SMBus™, and 1-Wire®, interfaces are all bidirectional, open-drain I/O topologies. I²C has three speed ranges: standard mode at ≤100kbps, fast mode at ≤400kbps, and high-speed mode at ≤3.4Mbps. Level translation for bidirectional buses is more difficult, because one must translate in both directions on the same data line. Simple topologies based on resistor-diode and single-stage-transistor translators with open collector or drain do not work because they are inherently unidirectional.

Unidirectional high- to low-level translation—input overvoltage tolerance

To translate from higher to lower logic levels, IC manufacturers produce a range of devices that are said to tolerate overvoltage at their inputs. A logic device is defined as input-overvoltage protected if it can withstand (without damage) an input voltage higher than its supply voltage. Such input-protected devices simplify the task of translating from higher- to lower-V_{CC} logic while increasing the signal-to-noise margin.

Overvoltage-tolerant inputs, for example, allow a logic device to cope with logic levels of 1.8V and higher while powered from a 1.8V supply. Devices in the LVC logic family, which are mostly input-overvoltage protected, work

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SMBus is a trademark of Intel Corp.
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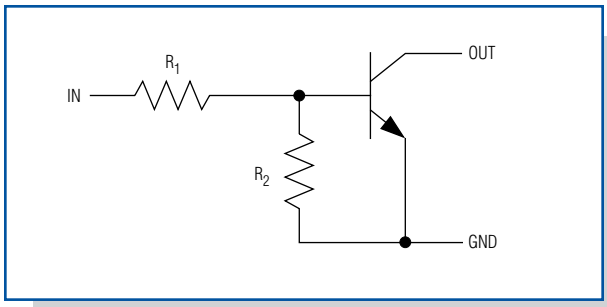

Figure 2. Using discrete/digital transistors is another alternative to bidirectional translation.

well in applications requiring high-to-low translations. The opposite situation of low-to-high translation is not as easy. It may not be feasible to generate higher voltage logic-level thresholds (V_{IH}) from lower voltage logic.

When designing a circuit for which connectors, high fanout, or stray load capacitance produce a high-capacitance load, you should remember that for all logic families, reducing the supply voltage also decreases the drive capability. An exception occurs between 3.3V CMOS or TTL (LV, LVT, ALVT, LVC, and ALVC) and 5V standard TTL (H, L, S, HS, LS, and ALS). In these logic families, the 3.3V and 5V logic activation points (V_{OL}, V_{IL}, V_{IH}, and V_{OH}) match each other.

Mixed high-low and low-high translation

Applications like the SPI bus require a mixture of high-low and low-high translation. Consider, for example, a processor at 1.8V and a peripheral at 3.3V. Though it is possible to mix techniques as described above, a single chip such as the MAX1840, MAX1841, or MAX3390 can implement the necessary translation by itself (**Figure 3**).

Other systems, such as I^2C and 1-Wire buses, require logic translation in both directions. Simple topologies, based on a single transistor with open collector or drain, do not work in a bidirectional bus because they are inherently unidirectional.

Bidirectional transceiver methods

For the larger byte- and word-wide buses where WR and RD signals already exist, one method for transferring data across the voltage levels is a bus switch such as the 74CBTB3384. Such devices are typically optimized for operation between 3.3V and 5V. For smaller 1- and 2-wire buses, this approach raises two issues. Firstly, it requires a separate enable pin to control the direction of data flow, and this ties up valuable port pins. Secondly, it requires large ICs that take up valuable board space.

All techniques have their pros and cons. Nonetheless, designers need a universal device that works across all translation levels, enables mixed low-to-high and high-to-low logic transitions, and includes unidirectional and/or bidirectional translation. A next-generation bidirectional level shifter (the MAX3370 in the MAX3370–MAX3393 family of ICs) fulfills those needs while overcoming some of the problems associated with alternative approaches.

The MAX3370, which implements a transmission-gate method of level translation (**Figure 4**), relies on external output drivers to sink current, whether they operate in a low-voltage or higher voltage logic domain. That

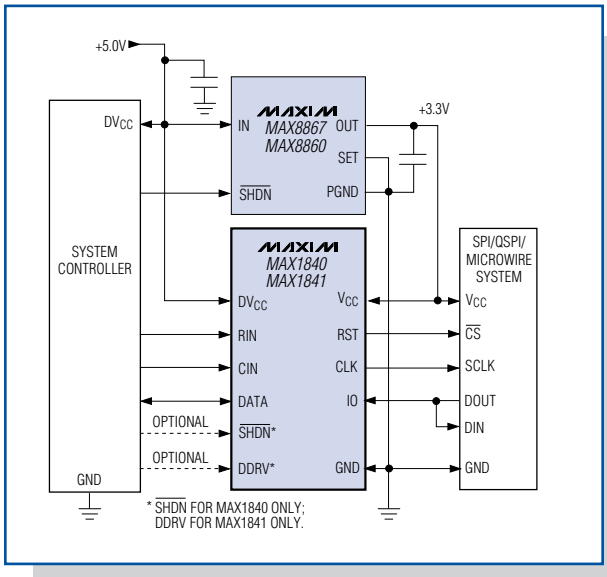

Figure 3. This diagram shows an example of an IC level translator with an SPI/QSPI™/MICROWIRE™ interface that can implement the necessary mixture of high-low and low-high translation.

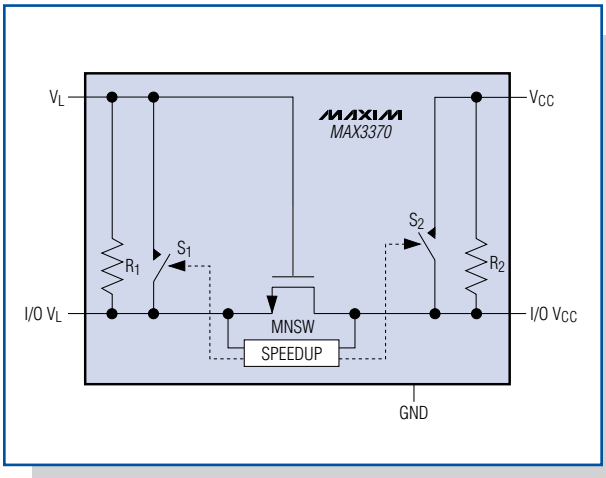

Figure 4. The MAX3370 implements a transmission-gate method of level translation.

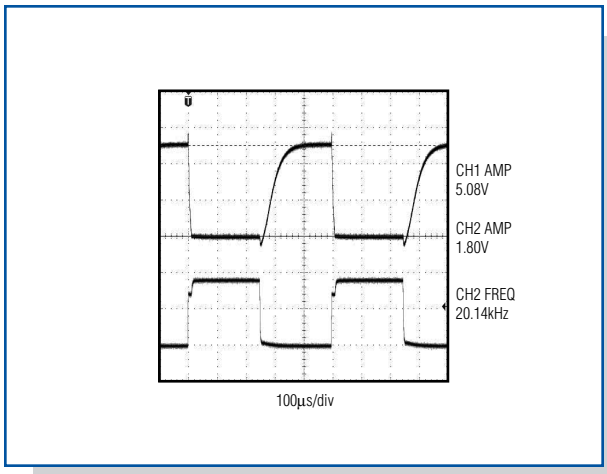

Figure 5. The scope plot of single FET open-drain output at 20kHz shows a limited effective data rate due to RC time constants.

capability enables the device to work with either open-drain or push-pull output stages. The relatively low on-resistance of a transmission gate (less than 135Ω), moreover, limits the speed of operation much less than the series resistor of Figure 1.

The design in Figure 4 offers two other advantages. Firstly, for open-drain topologies, the MAX3370 includes 10kΩ pull-up resistors paralleled by a "speed-up" switch. This minimizes the need for external pull-up resistors while reducing the RC time-constant ramp associated with traditional open-drain topologies. Secondly, the MAX3370's tiny SC70 package also conserves valuable board space.

Solving the speed problem

RC time constants limit the effective data rate for most other open-drain approaches (**Figures 5 and 6**). The MAX3370 IC family includes a patented speed-up scheme that actively pulls up rising edges, thereby minimizing the effect of capacitive loads as illustrated in **Figures 7, 8, and 9**. When the input goes above a predefined threshold, the device actively pulls up the rising edge, thereby minimizing any skew caused by external parasitic components. That capability can allow data rates as high as 20Mbps for signals produced by a push-pull driver. The speed of signals from open-drain drivers tends to be slower. As for other open-drain topologies, however, you can improve their speed by adding external pull-up resistors.

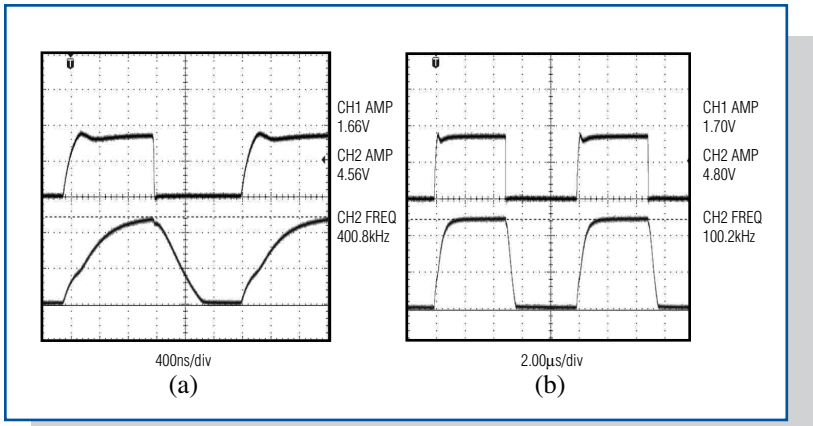

Figure 6. Scope plots of a dual-transistor transceiver translating 1.8V to 5V at 400kHz (a) and at 100kHz (b) illustrate limited effective data rates.

Solving the universal voltage problem

An application ideally requires a single component that can translate between any two logic levels at any speed. The ICs in the MAX337x family are designed for logic levels as low as 1.2V and as high as 5.5V. Consequently, this single component can provide the level translation required in most cases, without needing to select a logic device for each level-translator requirement.

Formerly, the need for low-to-high and high-to-low translations in the same circuit could be met only with separate chips. Now the bidirectional and topology-independent features (push-pull or open-drain) of a single chip from the MAX337x family solve both problems. The MAX3370 is a single-line, universal logic-level translator. For translating a larger number of I/O lines, consult the devices listed in **Table 1**.

As the number of I/O voltages per system increases, the need for level-translation techniques becomes more acute. Load capacitance, the magnitude of V_{CC} differences, and speed compound the problem. For high-to-low translation, the problem is less acute if the difference in translation voltages is minimal and off-the-shelf devices (such as logic ICs tolerant of input overvoltage) are available.

However, finding ICs and discrete-component circuits capable of handling ICs with wide differences in V_{CC} and of translating from low to high logic levels becomes difficult. Bidirectional and open-drain topologies do not lend themselves well to high-speed data rates. MAXIM's level translators ease the problem of level translation for a wide range of bi-/unidirectional, push-pull, and open-drain topologies. The ICs are available in ultra-small packages and require no external components for standard operation.

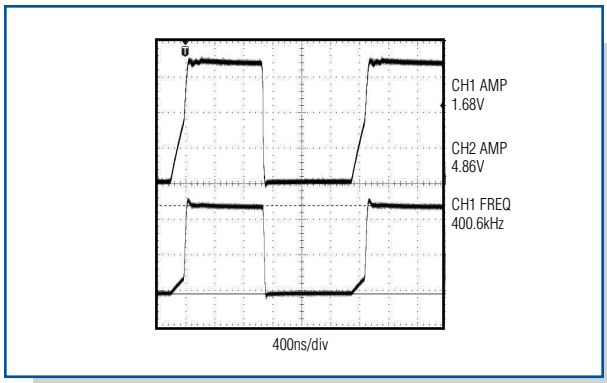

Figure 7. A scope plot of MAX3370 output with a translation of 1.8V to 5V at 400kHz shows minimized capacitive load effects.

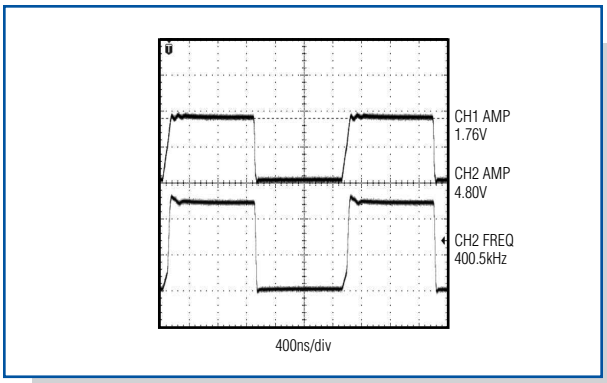

Figure 8. This scope plot of the MAX3370 output at 400kHz with 4.7kΩ pullup resistors shows the minimized effect of capacitive loads.

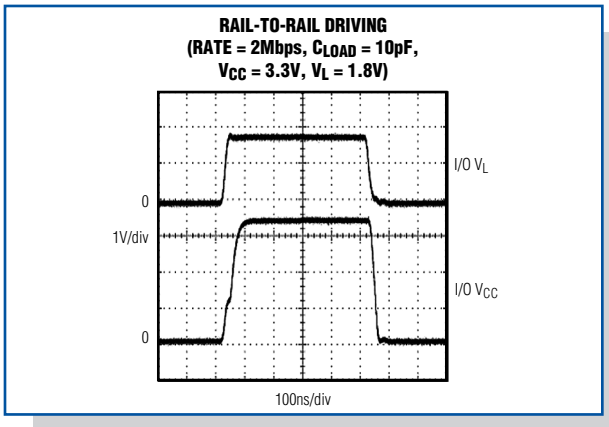

Figure 9. This plot shows an example of rail-to-rail driving of the output from a MAX3370 high-speed test circuit.

Table 1. Multiline logic-level translators

Part	No. of I/O Channels	Unidirectional/ Bidirectional Rx/Tx	V_L Range (V)	V_{CC} Range (V)	Separate Enable	Speeds Up to: (bps)
MAX3000/1	8	Bi, 8	1.2 to 5.5	1.65 to 5.5	Yes	230k/4M
MAX3002/3	8	Bi, 8	1.2 to 5.5	1.65 to 5.5	Yes	20M
MAX3013/23	8/4	Bi, 8/4	1.2 to (V_{CC} - 0.4)	1.65 to 3.6	Yes	100M
MAX3014–28	8	Uni, full mix	1.2 to (V_{CC} - 0.4)	1.65 to 3.6	Yes	100M
MAX3370/1	1	Bi, 1	1.65 to 5.5	2.5 to 5.5	No/Yes	2M
MAX3372/3	2	Bi, 2	1.2 to 5.5	1.65 to 5.5	Yes	230k
MAX3374 MAX3375 MAX3376	2	Uni, 2/0 Uni, 1/1 Uni, 0/2	1.2 to 5.5	1.65 to 5.5	Yes	16M
MAX3377/8	4	Bi, 4	1.2 to 5.5	1.65 to 5.5	Yes	230k
MAX3379	4	Uni, 4/0	1.2 to 5.5	1.65 to 5.5	Yes	16M
MAX3390	4	Uni, 3/1	1.2 to 5.5	1.65 to 5.5	Yes	16M
MAX3391	4	Uni, 2/2	1.2 to 5.5	1.65 to 5.5	Yes	16M
MAX3392	4	Uni, 1/3	1.2 to 5.5	1.65 to 5.5	Yes	16M
MAX3393	4	Uni, 0/4	1.2 to 5.5	1.65 to 5.5	Yes	16M
MAX13013/14	1/2	Bi, 1/2	1.2 to (V_{CC} - 0.4)	1.65 to 3.6	Yes	100M

IC drives up to four single-coil latching relays

Single-coil latching relays are found in applications including signal routing, audio, and automotive systems. These relays can pose a design challenge because coil current must flow in both directions through a single coil (**Figure 1**). Current flowing from pin 8 to pin 1 causes the relay to latch in its reset position, and current flowing from pin 1 to pin 8 latches the relay in its set position. The relay maintains its position even when the coil current is removed. Power is saved by removing coil current after the relay latches.

A simple circuit that drives up to four single-coil latching relays (**Figure 2**) includes a parallel-interface relay driver (U1) with open-drain outputs (**Figure 3**) and inductive-kickback protection. Latch any of the four relays to their set or reset positions by turning on the corresponding output (OUTX). That output is selected by asserting its digital address on pins A2 to A0 while $\overline{CS}$ is high. Activate the output by toggling $\overline{CS}$ (**Figure 4**).

Current flows into the enabled open-drain output and latches the relay to its set or reset position, according to the direction of the coil current. Drive $\overline{RESET}$ low to turn off all enabled open-drain outputs, as soon as the relays latch to ensure lowest power consumption. Observe the set/reset timing shown in Figure 4. Do not pull $\overline{RESET}$ low until the required time ($t_{SET/RESET}$) has elapsed. Waiting $t_{SET/RESET}$ after the last $\overline{CS}$ toggle ensures that all selected relays will properly latch to their intended positions.

Clamping diodes on each OUTX pin catch high-voltage transients that occur when the coil current is interrupted. Those diodes, as shown in Figure 2, clamp the OUTX voltage at V_{CC} - 0.7V.

A similar article appeared in the February, 2004 issue of EET.

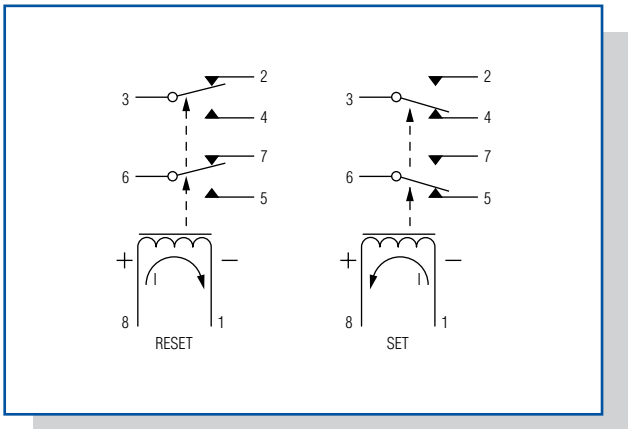

Figure 1. Current flow in a single coil latches the corresponding relay in its SET or RESET position.

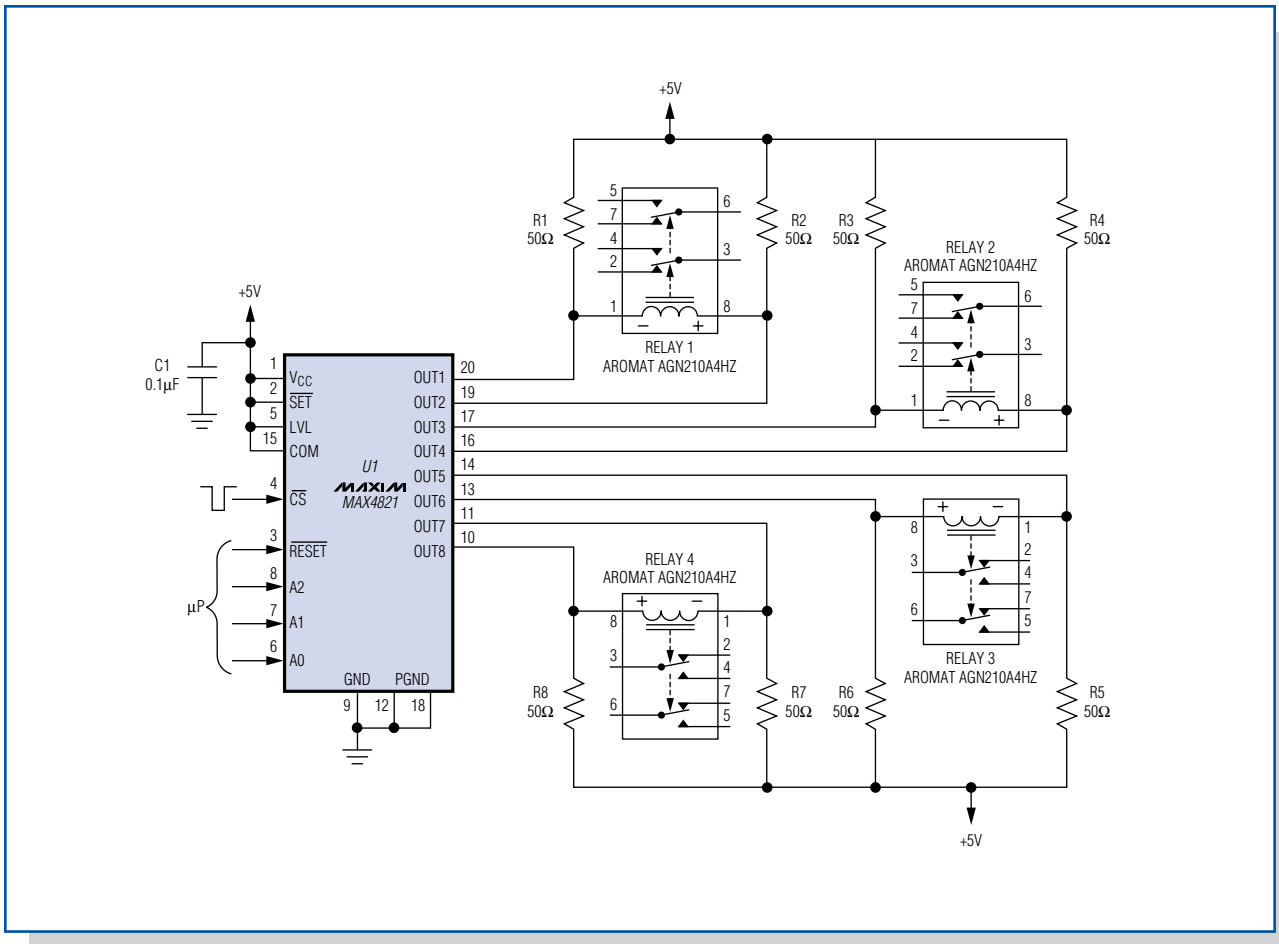

Figure 2. This circuit easily drives four, single-coil latching relays.

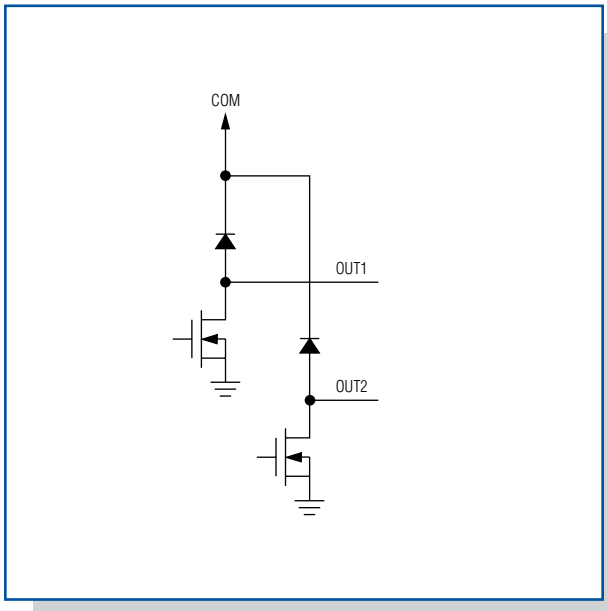

Figure 3. This diagram shows two of the eight open-drain outputs from the circuit of Figure 2.

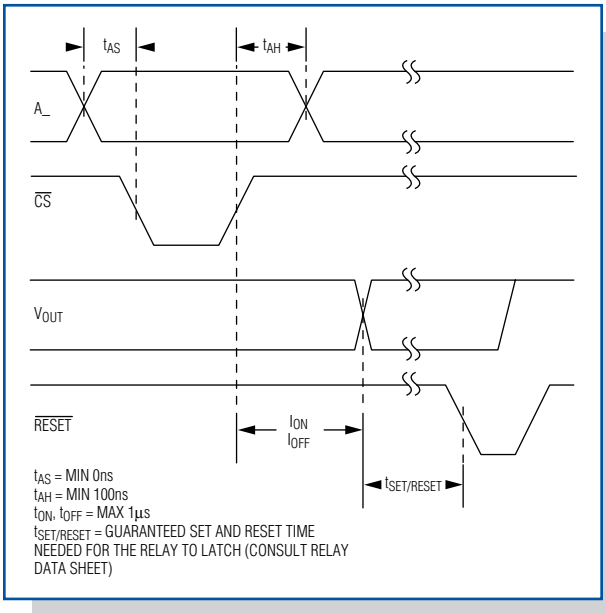

Figure 4. Interface timing for the circuit in Figure 2 illustrates the activated output.

Supervisor IC indicates fan failure

The brushless DC fans found in many types of equipment can be crucial to the performance and longevity of that equipment. A quick indication of fan failure, moreover, can be essential in preventing major damage. Among the many approaches for identifying and indicating stalled fans, the circuit of **Figure 1** is very simple and reliable.

The fan's tachometer output connects to the watchdog input of a µP supervisor (U1). The LED remains off during normal operation. If the tachometer does not change state within a watchdog timeout period, U1 lights the LED by asserting its reset output. As a result, the LED pulses on and off as the supervisor goes through its watchdog/reset cycle. The LED in this example has a 200ms on-time and flashes with a period of 1.6s, which is suitable for most purposes.

A similar article appeared in the November, 2003 issue of EET.

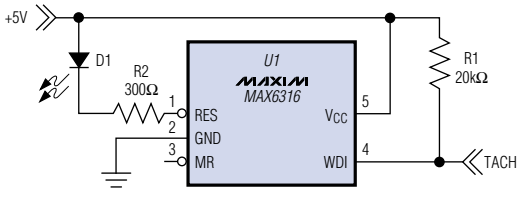

Figure 1. The MAX6316 µP supervisor monitors a fan's tachometer output.

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